

REMARKS

Introduction

Claims 1-4, 15-18, and 28-33 are pending in the above-identified patent application.

Claims 1-4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sharrit et al. U.S. Patent No. 5,999,990 (hereinafter "Sharrit") in view of Vernon et al. European Patent No. EP 0 801 351 A2 (hereinafter "Vernon"). Claim 15 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Kean U.S. Patent No. 5,705,938 (hereinafter "Kean '938") in view of Kean U.S. Patent No. 5,469,003 (hereinafter "Kean '003"). Claims 16-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kean '938 in view of Kean '003 and further in view of Vernon. Claim 28 was rejected under 35 U.S.C. § 102(e) as being anticipated by Sharrit.

Claims 29-33 were objected to as being dependent upon rejected base claim 28.

Reconsideration of this application in light of the following remarks is hereby respectfully requested.

Claims 1-4

Claims 1-4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sharrit in view of Vernon. The Examiner's rejections are respectfully traversed.

The Examiner concedes that Sharrit "does not expressly disclose about at least one programmable logic resource that is at least partially configured as a central processing unit." To make up for this deficiency, the Examiner states that "Vernon explicitly discloses implementing at least one programmable logic resource as a central processing unit." Office Action, p. 4, ¶ 7.

Applicants respectfully submit that, in addition to the above deficiency, Sharrit further fails to show or suggest "a secondary storage device that stores configuration data for the programmable logic" as recited in applicants' independent claim 1.

The Examiner cites col. 5, lines 33-57 of Sharrit as showing the secondary storage device. This portion of Sharrit refers to FIG. 2, which shows a reconfigurable resource unit (RRU) that includes a digital signal processor (DSP) coupled to a random access memory (RAM). The RRU can also include a mass storage unit such as a hard disk drive (HDD) that stores

a library of programs to be executed in the DSP. Sharrit, FIG. 2; and col. 5, lines 33-57.

According to Sharrit, the hard disk drive stores programs that are executed by the DSP, and does not store configuration data for programmable logic as recited in applicants' independent claim 1. More particularly, programs that are executed by the DSP must be software programs that are based on the instruction set hard-wired in the DSP. There is no way in which configuration data that is used to program programmable logic can be used by the DSP according to Sharrit.

Likewise, Vernon also fails to show or suggest the secondary storage device that stores configuration data as recited in applicants' independent claim 1.

Because neither Sharrit nor Vernon, whether taken alone or in combination, show or suggest all the features of applicants' independent claim 1, applicants respectfully submit that claim 1 is allowable. Claims 2-4, which depend from claim 1, are also allowable.

Claims 15-18

Claim 15 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Kean '938 in view of Kean '003.

Claims 16-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kean '938 in view of Kean '003 and further in view of Vernon. The Examiner's rejections are respectfully traversed.

Applicants have amended independent claim 15 to more particularly define the claimed invention. No new matter has been added and the amendment is fully supported by the originally-filed specification (see, e.g., applicants' specification, p. 5, lines 21-29; and p. 14, lines 1-17).

The Examiner concedes that Kean '938 "does not expressly disclose that the external memory is a mass storage device." To make up for this deficiency, the Examiner relies on Kean '003, which the Examiner alleges "clearly discloses ... storing the configuration data in a disk file." Office Action, p. 6, ¶ 12.

Regardless of whether Kean '938 or Kean '003 show an external memory that is a mass storage device, neither Kean '938 nor Kean '003 show or suggest "automatically swapping configuration data between a secondary storage device and the programmable logic resources during programmable logic resource allocation using a virtual logic manager" as recited by applicants' independent claim 15.

Kean '938 refers to a programmable switch for a

field programmable gate array (FPGA) that allows a user to reconfigure or partly reconfigure the FPGA. Kean '938, Abstract. According to Kean '938, a snapshot of the state of the FPGA including configuration information and the state of registers is taken and saved in an external memory ("swapping in"), the FPGA is reconfigured to perform another task, and the snapshot of the state of the FPGA from the external memory is then restored ("swapping out"). Kean '938, col. 11, line 49 to col. 12, line 54.

Kean '938 fails to show or suggest using a virtual logic manager in connection with the "swapping in" and "swapping out" of configuration data. More particularly, applicants' invention, as defined by independent claim 15, uses a virtual logic manager to automatically swap configuration data between programmable logic resources and a mass storage device. Kean '938, however, makes no mention of using a virtual logic manager, which is defined as being responsible for the run-time allocation of programmable logic devices by managing the run-time swapping of functions to be implemented in programmable logic according to applicants' specification (applicants' specification, p. 13, lines 23-34). Further, it appears that the "swapping" of Kean '938 is accomplished through a pre-programmed routine of a user

application that predetermines when and what is swapped in and out.

Applicants respectfully submit that Kean '003 also does not show or suggest this feature of applicants' independent claim 15.

Therefore, neither Kean '938 nor Kean '003, whether taken alone or in combination, show or suggest all the features of applicants' independent claim 15.

Moreover, applicants respectfully submit that the Examiner has failed to provide any suggestion or motivation to combine Kean '938 with Kean '003 to show all the features of applicants' independent claim 15. In fact, applicants respectfully submit that Kean '938 teaches away from being combined with Kean '003. For example, Kean '938 describes allowing a user to specify user logic to reconfigure an FPGA, while Kean '003 describes a processor that uses configuration data stored in a disk file or non-volatile memory to reconfigure an FPGA.

Because neither Kean '938 nor Kean '003, whether taken alone or in combination, show or suggest all the features of applicants' independent claim 15, because the Examiner has failed to point to a suggestion or motivation to combine Kean '938 with Kean '003 to show all the features of

applicants' independent claim 15, and because, in fact, Kean '938 teaches away from being combined with Kean '003 to show all the features of applicants' independent claim 15, applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness (MPEP § 2142).

For at least the foregoing reasons, independent claim 15 is allowable. Claims 16-18, which depend from claim 15, are also allowable.

Claims 28-33

Claim 28 was rejected under 35 U.S.C. § 102(e) as being anticipated by Sharrit. Claims 29-33 were objected to as being dependent upon rejected base claim 28. The Examiner's rejection and objections are respectfully traversed.

Applicants respectfully submit that Sharrit fails to show or suggest "during run-time, using a virtual computer operating system to autonomously determine whether to use a hardware implementation or a software implementation for a given one of the multiple functions of the given application" as recited in applicants' independent claim 28.

According to Sharrit, the determination of whether to process data in either hardware or software is pre-defined

based on the configuration files used to reconfigure an RRU, and is not autonomously determined during run-time as recited in applicants' independent claim 28. More particularly, Sharrit describes a hybrid RRU having both hardware and software capability, in which data from the configuration files are used indicate whether the configuration files are processed in the hardware (in FPGA) or in the software (in DSP). Sharrit, col. 1, lines 54-64; col. 2, lines 35-45; and col. 6, lines 23-35 and 54-57.

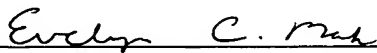
For at least the foregoing reason, independent claim 28 is allowable. Claims 29-33, which depend from claim 28, are also allowable.

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Conclusion

Applicants respectfully submit that this application is in condition for allowance. Accordingly, prompt consideration and allowance of this application are respectfully requested.

Respectfully submitted,



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